Theory and Design of an Ultra-Linear Square-Law Approximated LDMOS Power Amplifier in Class-AB Operation

Mark P. van der Heijden, *Student Member, IEEE*, Henk C. de Graaff, *Member, IEEE*, Leo C. N. de Vreede, *Member, IEEE*, John R. Gajadharsing, and Joachim N. Burghartz, *Fellow, IEEE*

***Abstract*—This paper describes a power amplifier, employing parallel-connected laterally diffused metal–oxide semiconductor (LDMOS) devices with optimized channel widths and bias offsets to approximate ideal square-law behavior of the overall transconductance in class-AB operation. The proposed method results in a significant linearity improvement over a large dynamic range in comparison to a conventional amplifier in class-A or class-AB operation. Measurements demonstrate an improvement of 20 dB in third-order intermodulation distortion and 10 dB in adjacent channel power ratio for wide-band code-division multiple access at 12-dB output power backoff from the 1-dB gain compression point. Consequently, this amplifier can be operated more toward the compression region with better linearity and drain efficiency compared to a conventional LDMOS power-amplifier design.**

***Index Terms*—AM–AM, AM–PM, base stations, efficiency, intermodulation distortion, LDMOS, linearization, power amplifiers.**

I. Introduction

LINEARITY is one of the major aspects in base-station RF-power amplifier design. Currently, laterally diffused metal–oxide semiconductor (LDMOS) is the technology of choice in this market, providing high gain and good linearity compared to other semiconductor technologies [1]. However, the stringent linearity requirements for the new complex modulation schemes, like wide-band code-division multiple access (WCDMA) still require an LDMOS-based amplifier to be operated 10–13 dB below the 1-dB gain compression point (P1dB). When considering the requirements for driver stages, the situation is even worse. For these amplifiers, typically a class-A operation is needed in order to meet the linearity specifications. This is in spite of their inherent lower efficiency and larger active die areas needed to provide the desired output power.

To improve on both linearity and efficiency, several linearization techniques have been developed, such as feed-forward and adaptive predistortion [2], [3]. The complexity of these solutions generally results in large space consumption on the printed circuit board, a long design time, and high cost. In this paper, we will discuss a linearization method yielding a considerable reduction in intermodulation distortion (IMD) and adjacent channel power ratio (ACPR) for FET power amplifiers without significantly increasing circuit complexity. To accomplish this from a device point-of-view, Sections II and III provide the theory and technique for square-law approximation of the drain current ($I_{\rm DS}$) versus gate voltage ($V_{\rm GS}$) relationship near the cutoff region [4]. This proves to be essential in obtaining high linearity over a wide dynamic range in class-AB operation of the amplifier. Note that the proposed linearization technique differs from conventional techniques since the linearization is incorporated in the device core of the amplifier itself, rather than by separate circuit solutions. To optimize the relatively large number of design parameters involved, Section IV discusses a dedicated linearity optimization protocol developed for this purpose. This optimization protocol is based on the minimization of AM–AM conversion (modulation of output signal amplitude as function of input signal amplitude) and AM–PM conversion (modulation of output signal phase as function of input signal amplitude) and relates the IMD to the large-signal S_{21} as function of power using the complex power series representation (CPSR) [5], [6]. Consequently, full amplifier characterization of gain and linearity is combined in a single instrument (network analyzer) test setup and speeds up the optimization process considerably. Finally, Section V compares the measurement results of the ultra-linear class-AB LDMOS power amplifier against the stringent specifications of third-generation (3G) wireless networks.

II. Linear Operation of Class-AB Amplifiers

In conventional RF power-amplifier configurations, the loading conditions and bias operation point of the active device both control the linearity of the complete amplifier [2]. In LDMOS experiments [1], it has been demonstrated that, for a class-AB operation, the choice of the quiescent bias point determines the amplifier linearity in the backoff region. In fact, a sharp optimum for the third-order intermodulation (IM3) product exists for a particular gate-bias voltage, yielding a rather linear gain characteristic over a wide dynamic range.

In order to develop required theory and linearization tools for ultra-linear LDMOS power amplifiers, IM3 is analyzed as a function of power using a power series analysis [2]. This approach provides the required insight for the device linearity in

Manuscript received October 15, 2001. This work was supported by Philips Semiconductors.

M. P. van der Heijden, H. C. de Graaff, L. C. N. de Vreede, and J. N. Burghartz are with the Department of Information Technology and Systems, Laboratory of Electronic Components Technology and Materials, Delft Institute of Microelectronics and Submicron Technology, Delft University of Technology, 2628 CT Delft, The Netherlands (e-mail: M.P.vanderHeijden@its.tudelft.nl).

J. R. Gajadharsing is with Business Line RF Modules, Philips Semiconductors, Nijmegen, The Netherlands.

Publisher Item Identifier 10.1109/TMTT.2002.802332.

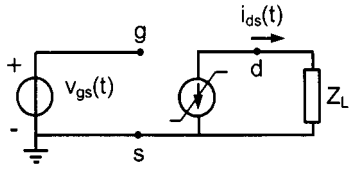

Fig. 1. Strongly simplified model of an LDMOS device.

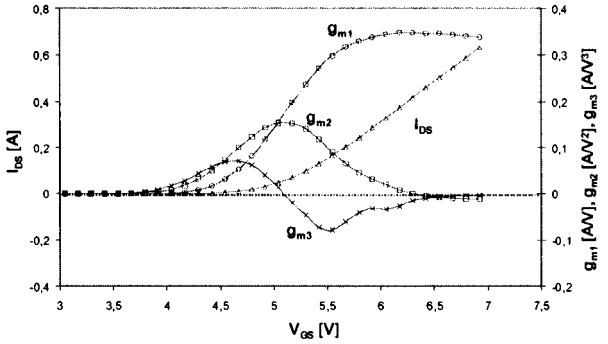

Fig. 2. Measured $I_{\rm DS}$ versus $V_{\rm GS}$ characteristic of a 12-mm LDMOS FET and its derived Taylor coefficients versus $V_{\rm GS}$ at a drain voltage $V_{\rm DS} = 26$ V.

class-AB operation. Fig. 1 shows a strongly simplified LDMOS model used for the analysis. Note that this model assumes that the input power is directly related to the voltage at the gate. Furthermore, the model only takes into account the predominant source of distortion in an FET amplifier, i.e., the nonlinear $I_{\rm DS}$–$V_{\rm GS}$ relationship [7], [8]. This can be modeled by means of a Taylor series expansion around the bias point $V_{\rm GS}$ as follows:

$$\begin{aligned} i_{\rm ds}(t) &= \left.\frac{dI_{\rm DS}}{dV_{\rm GS}}\right|_{V=V_{\rm GS}} v_{\rm gs}(t) + \frac{1}{2!}\left.\frac{d^2I_{\rm DS}}{dV_{\rm GS}^2}\right|_{V=V_{\rm GS}} v_{\rm gs}^2(t) \\ &\quad + \frac{1}{3!}\left.\frac{d^3I_{\rm DS}}{dV_{\rm GS}^3}\right|_{V=V_{\rm GS}} v_{\rm gs}^3(t)\ldots \\ &= g_{m1}v_{\rm gs}(t) + g_{m2}v_{\rm gs}^2(t) + g_{m3}v_{\rm gs}^3(t) + g_{m4}v_{\rm gs}^4(t) \\ &\quad + g_{m5}v_{\rm gs}^5(t)\ldots. \end{aligned} \tag{1}$$

Fig. 2 shows the $I_{\rm DS}$–$V_{\rm GS}$ relationship and its derived Taylor coefficients of a Philips LDMOS device with a gatewidth $W = 12$ mm at a typical drain voltage ($V_{\rm DS} = 26$ V) used in base stations. In order to obtain a behavioral model of the drain current source, we have fitted a thirteenth-order polynomial function to the third derivative (g_{m3}) of the measured $I_{\rm DS}$ versus $V_{\rm GS}$, ranging from 4.0 to 5.8 V. Fig. 3 shows this function together with g_{m1} and g_{m5}, which are calculated by integration and derivation, respectively. By substituting a two-tone signal $v_{\rm gs}(t) = V_S(\cos\omega_1 t + \cos\omega_2 t)$ into (1), we obtain power series expressions at frequency components throughout the spectrum [2]. Hence, the magnitude of IM3 as function of input voltage (V_S) can be expressed as the quotient of the nonlinear current at the intermodulation frequency $i_{{\rm ds},(2\omega_1-\omega_2)}$ and the nonlinear current at the fundamental frequency $i_{{\rm ds},\omega_1}$ as follows:

$$\text{IM3} = \left|\frac{i_{{\rm ds},(2\omega_1-\omega_2)}}{i_{{\rm ds},\omega_1}}\right| = \left|\frac{\frac{3}{4}g_{m3}V_{\rm S}^3 + \frac{25}{8}g_{m5}V_{\rm S}^5}{g_{m1}V_{\rm S} + \frac{9}{4}g_{m3}V_{\rm S}^3 + \frac{25}{4}g_{m5}V_{\rm S}^5}\right|. \tag{2}$$

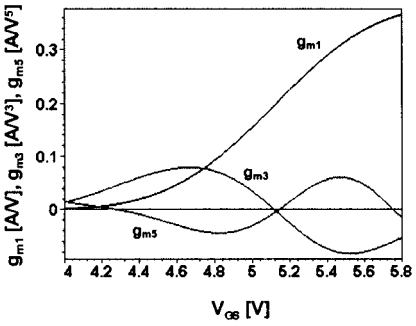

Fig. 3. Modeled g_{m1}, g_{m3}, and g_{m5} of a 12-mm LDMOS FET at $V_{\rm DS} = 26$ V.

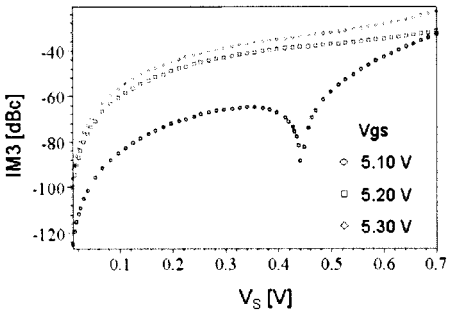

Fig. 4. Predicted IM3 versus input amplitude $V_{\rm S}$ of the two-tone signal as calculated by (2).

Note that (2) only contains odd-order Taylor coefficients and its numerator indicates which terms should be minimized to obtain the highest amplifier linearity. Due to the fact that the numerator depends on the *order* of the power series analysis applied, it is essential for a reasonable power range to include at least terms up to the fifth degree [9]. In the following, we will use (2) to investigate the relation between the gate bias voltage and the IM3 distortion level as function of input power.

If we consider the modeled odd-order Taylor coefficients shown in Fig. 3, we can observe that g_{m3} and g_{m5} become zero close to $V_{\rm GS} = 5.1$ V. According to (2), this will result in minimum IM3 as function of input voltage amplitude $V_{\rm S}$, while IM3 will be higher for other values of $V_{\rm GS}$. To illustrate this, Fig. 4, shows a low IM3 versus $V_{\rm S}$ relationship at $V_{\rm GS} = 5.1$ V. On the other hand, exact cancellation of IM3 will only occur at a particular value of $V_{\rm S}$ if the contributions of the third- and the fifth-order components are equal and have opposite signs. What we actually want is an overall decrease in IM3 independent of $V_{\rm S}$, which can only be obtained theoretically if all the higher odd-order Taylor coefficients are zero. In support of this theory, Fig. 5 shows the measured IM3 versus output power of the 12-mm device at different gate-bias voltages. It demonstrates that IM3 has indeed an optimum for low powers at $V_{\rm GS} = 5.1$ V, which is in agreement with our foregoing analysis. In comparison with the class-AB IM3 results in Fig. 5, the IM3 in class-A operation yields superior linearity in the low-power range. This is because, in a class-A bias condition (around $V_{\rm GS} = 6.5$ V), all the higher order Taylor coefficients tend to go to zero (see Fig. 2) and favors the current use of class-A driver stages in LDMOS.

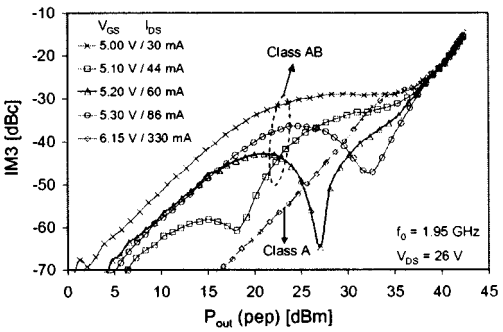

Fig. 5. Measured IM3 versus peak-envelope output power for a conventional class-AB LDMOS power amplifier at $f = 1.95$ GHz and $\Delta f = 200$ kHz for different gate-bias conditions.

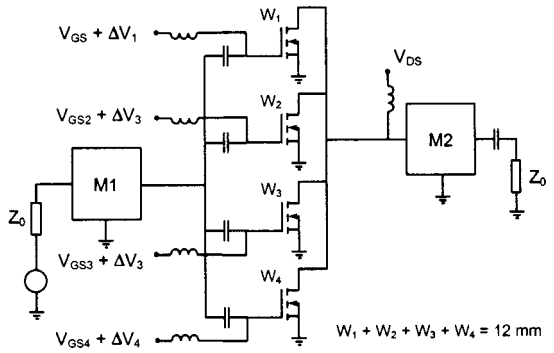

Fig. 6. Distributed amplifier design using four parallel LDMOS devices with different gatewidths and gate bias.

In conclusion, the previous analysis indicates that, in a bias point-of-view, the best class-AB power-amplifier linearity is obtained if its odd-order derivatives (g_{m3} and g_{m5}, etc.) are small and g_{m1} is reasonably large. Section III will exploit this feature in a novel LDMOS power-amplifier design.

III. Theory of a Novel Class-AB FET Power-Amplifier Design

The specifications for wide-band code-division multiple-access (WCDMA) base-stations demand that the power amplifier must handle signals with a large peak-to-average ratio (crest factor), typically of 10 dB [10]. We can interpret this for having a low IM3 as function of input power in the output power backoff (OPBO) region ($<$ 10 dB). As discussed in Section II, we found an optimum bias point related to the odd-order Taylor coefficients of the transconductance nonlinearity, yielding a low IM3 as function of power in the OPBO region. Consequently, a further linearity improvement can be obtained by adjusting the shape of the transconductance as a function of $V_{\rm GS}$.

In previous work, the derivative superposition (DS) method has been proposed to minimize the IM3 of a class-A amplifier using parallel-connected high electron-mobility transistor (HEMT) or MESFET devices [8], [11]. DS is based on the canceling of g_{m3} itself rather than the minimization of the numerator of (2). More recent work on multiple gated RF CMOS devices [12] again only focuses on the minimization of g_{m3} versus gate voltage. Note, however, that the power or Volterra-series analysis approach is, in principal, only valid at a single bias point and that statements about IMD versus signal power should always take into account the higher order derivatives (> 3) of the nonlinearity. This is especially true when the device is operated in a highly nonlinear region like the cutoff region of a MOSFET [2]. Consequently, in the case of our class-AB amplifier, focus must be placed on the lowering of the total contributions of g_{m3}, g_{m5}, etc. with respect to (2) in order to achieve a linearity improvement over a wide dynamic range. In fact, by doing this, we approximate the square-law behavior of the $I_{\rm DS}$-$V_{\rm GS}$ current relationship in the class-AB (cutoff) bias region. The DS method will be employed as a tool to create the desired characteristic. Ideally, the best approximation would include an infinitively large amount of devices placed in parallel, but for practical reasons, we will limit ourselves to four.

Fig. 6 shows a schematic circuit implementation of this technique, in which four LDMOS FETs are placed in parallel. For each of these devices, the variables are the gatewidths (W_n) and the gate-bias offsets (ΔV_n) with respect to $V_{\rm GS}$ to control the transconductance behavior. $M1$ and $M2$ are matching networks and Z_0 is the characteristic impedance. The total gatewidth $W = W_1 + W_2 + W_3 + W_4 = 12$ mm, which equals the width of the single reference LDMOS device. For the analysis, we assume that the total drain current can be modeled as a single current source, which is expressed as

$$I_{\rm DS,tot} = \frac{W_1}{12} I_{\rm DS}\left(V_{\rm GS} + \Delta V_1\right) + \frac{W_2}{12} I_{\rm DS}\left(V_{\rm GS} + \Delta V_2\right) + \frac{W_3}{12} I_{\rm DS}\left(V_{\rm GS} + \Delta V_3\right) + \frac{W_4}{12} I_{\rm DS}\left(V_{\rm GS} + \Delta V_4\right). \tag{3}$$

In this equation, $I_{\rm DS}(V_{\rm GS})$ is the model of the drain current source of the 12-mm LDMOS device described in Section II. Again, we break down our Taylor-series expansion after the fifth term and only consider the following odd terms:

$$i_{\rm ds,tot}(t) = g_{m1,\rm tot} v_{\rm gs}(t) + g_{m3,\rm tot} v_{\rm gs}^3(t) + g_{m5,\rm tot} v_{\rm gs}^5(t). \tag{4}$$

The Taylor coefficients $g_{mk,\rm tot}$ (k is a positive odd integer) depend on $W_1 - W_4$ and the bias offsets $\Delta V_1 - \Delta V_4$, shown in (5), at the bottom of this page. If we now substitute this expression in (2), we get an expression for IM3, which depends on $W_1 - W_4$ and $\Delta V_1 - \Delta V_4$ and $V_{\rm GS}$. The complete model was optimized manually in MAPLE [13] by lowering g_{m3} and g_{m5} versus $V_{\rm GS}$ to obtain a square-law approximated $I_{\rm DS}$–$V_{\rm GS}$ relationship and low IM3 versus input signal $V_{\rm S}$. The gatewidths of the devices are $W_1 = 3$ mm, $W_2 = 2$ mm, $W_3 = 2$ mm,

$$g_{mk,\rm tot} = \frac{1}{k!} \left. \frac{d^k I_{\rm DS,tot}\left(W_1, W_2, W_3, W_4, \Delta V_1, \Delta V_2, \Delta V_3, \Delta V_4, V_{\rm GS}\right)}{dV_{\rm GS}^k} \right|_{V = V_{\rm GS}} \tag{5}$$

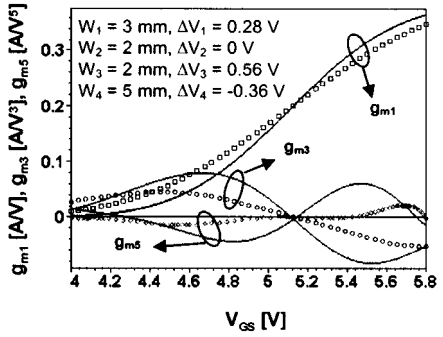

Fig. 7. Modeled odd-order Taylor coefficients of the single 12-mm (solid lines) and optimized distributed LDMOS device (dotted lines).

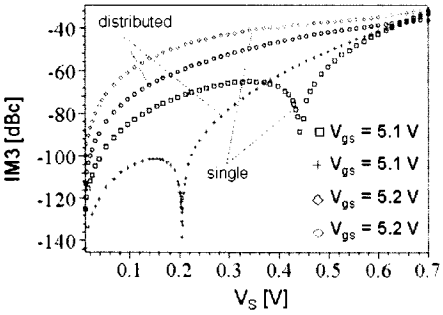

Fig. 8. Predicted IM3 versus $V_{\rm S}$ of the single (see Fig. 4) and optimized distributed device at two different bias conditions, as calculated by (2).

and $W_4 = 5$ mm and the bias offsets are $\Delta V_1 = 0.28$ V, $\Delta V_2 = 0$ V, $\Delta V_3 = 0.56$ V, and $\Delta V_4 = -0.36$ V, respectively. We also observe that some devices are individually biased more toward class A and some more toward class B. Fig. 7 shows the odd-order Taylor coefficients g_{m1}, g_{m3}, and g_{m5} of the reference device (see Fig. 3) together with those of the optimized distributed[1] device. Fig. 8 shows the predicted IM3 versus $V_{\rm S}$ for the optimized distributed device and the reference device for two situations. First, both the devices are biased in the zero crossing of g_{m3} to obtain the lowest distortion at small-signal levels. Secondly, both the devices are biased 0.1 V above the zero crossing to show that the relative improvement of IM3 does not only occur at a single-bias condition. However, the improvement is more pronounced when the devices are biased near the zero crossing.

Note that the model used in the foregoing analysis is a simplified view of reality; in practice, other nonlinearities (like $C_{\rm GS}$, $C_{\rm DS}$, and $R_{\rm DS}$) will also contribute to the distortion properties of the amplifier. For this reason, proper selection of the gate-bias voltages proves to be a nontrivial task using the previously discussed model. Until now, the amplifier is operated in the pre-compression region (10–12-dB OPBO) where the transconductance nonlinearity is dominant. However, if the amplifier is operated closer to compression, the influence of $R_{\rm DS}$ and $C_{\rm DS}$ also becomes notable, yielding severe AM–AM and AM–PM conversion. With respect to $C_{\rm GS}$, we have found from simulations that the distributed device concept also yields improvement for the AM–PM conversion in the pre-compression region. The design problem is now to find the optimum parameters ($W_1 - W_4$ and $\Delta V_1 - \Delta V_4$), which give the best overall linearity improvement in the OPBO region. In order to overcome these difficulties and find the optimum values of the relative large number of design parameters, we have developed a linearity optimization routine to obtain the desired amplifier linearity in the experiment. The proposed method is based on the CPSR and is discussed in Section IV.

[1]The term "distributed device" will be used in the remainder of this paper in the sense that it is comprising of parallel-connected devices having a gatewidth equal to the gatewidth of the single reference device of 12 mm.

IV. Experimental Determination of the Design Parameters

This section describes an optimization method for linearity in terms of IMD by minimizing AM–AM and AM–PM conversion. IMD can be related to AM–AM and AM–PM conversion by means of the CPSR [6]. To justify this approach with respect to the analysis in Sections II and III, we examine the AM–AM conversion using our simplified power series analysis by substituting a single-tone signal $v_i(t) = V_S \cos(\omega_0 t)$ in (1). This yields an output signal at the fundamental frequency ω_0 [2] as follows:

$$i_{{\rm ds},\omega_0}(t) = \left[g_{m1}V_s + \frac{3}{4}g_{m3}v_s^3 + \frac{5}{8}g_{m5}V_s^5\right]\cos(\omega_0 t). \quad (6)$$

The term in square brackets represents the AM–AM conversion as function of the input signal amplitude $V_{\rm S}$. Consequently, (6) contains all the odd-order Taylor coefficients, which also determine IM3 in (2) motivating the use of the CPSR. In a similar way, charge nonlinearities ($C_{\rm GS}$) are automatically included in the AM–PM conversion.

A. CPSR Model for IM3 Calculation

The CPSR described in [6] assumes that the amplifier does not have memory effects related to the time constant of the IF component $\omega_1 - \omega_2$ in a two-tone test. This frequency component causes bias modulation and should be properly terminated [2], [14], [15]. Furthermore, the CPSR assumes the passband of the amplifier to be relatively narrow with a constant frequency response. In practical amplifiers for wireless telecommunication, these conditions are met and IM3 is completely characterized by the AM–AM and AM–PM conversion.

Our method for determining IM3 can be outlined as follows. First, we obtain AM–AM and AM–PM conversion by measuring S_{21} versus input power using a vector network analyzer (VNA) and rewrite the CPSR model to fit the data. Secondly, we obtain the required CPSR coefficients using a least square method. Lastly, we compute the IM3 as function of power up to the gain compression region using the CPSR model. Fig. 9 shows a black-box representation of the power amplifier used in the following analysis.

1) Characterizing AM–AM and AM–PM Conversion: Equation (7) formulates the general expression for the complex power series in terms of voltage [6]

$$v_o(t) = a_1 v_i(1-\tau) + {\rm Re}\left[\sum_{n=3}^{N}\vec{a}_n\left\{v_i^n(t-\tau) + jH\left[v_i^n(t-\tau)\right]\right\}\right]. \quad (7)$$

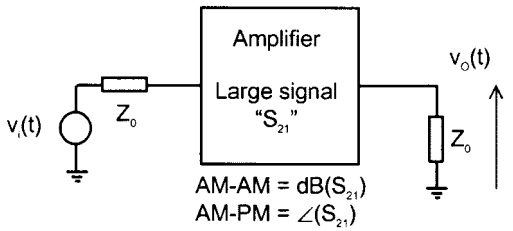

Fig. 9. Black-box representation of a nonlinear amplifier characterized by its AM–AM and AM–PM conversion.

In this equation, $v_i(t)$, $v_0(t)$ are the input and output voltage related to $Z_0 = 50\ \Omega$, a_1 is the linear voltage gain, $\vec{a}_n = R_n e^{j\phi_n}$ are the complex coefficients, $H[v_i^n(t)]$ is the Hilbert transform of $v_i(t)$, τ is the delay time of the amplifier, and n is a *positive odd* integer. In order to relate the AM–AM and AM–PM conversion to the model in (7), we substitute a single sinusoid $v_i(t) = V_s \cos(\omega_0 t)$ in (7) and set τ to zero since we are only interested in deviations of the phase response. Now, (8) yields the generalized expression of the amplifier output voltage $v_0(t)$ at the fundamental frequency besides other spectral components. We do not consider these components since all the information for odd-order distortion is enclosed by the AM–AM and AM–PM conversion

$$\begin{aligned} v_{o,\omega_0}(t) &= \left[a_1 V_S + \sum_{n=3}^{N} \frac{1}{2^{n-1}} \left(\frac{n+1}{2}\right) V_S^n R_n \cos\phi_n\right] \cos\omega_0 t \\ &\quad - \left[\sum_{n=3}^{N} \frac{1}{2^{n-1}} \left(\frac{n+1}{2}\right) V_S^n R_n \sin\phi_n\right] \sin\omega_0 t \end{aligned} \tag{8}$$

in which $\binom{n}{r} = n!/r!(n-r)!$ is the binomial coefficient. This trigonometric expression is rewritten in its more convenient form, as expressed in (9), as follows:

$$\begin{aligned} v_{o,\omega_0}(t) &= a_1 V_S R(V_S)\Big\{\cos\left[\Psi(V_S)\right]\cos\omega_0 t - \sin\left[\Psi(V_S)\right]\sin\omega_0 t\Big\} \end{aligned}$$

or

$$v_{o,\omega_0}(t) = a_1 V_S R(V_S) \cos\left\{\omega_0 t + \Psi(V_S)\right\} \tag{9}$$

where

$$R(V_S)\sin\left[\Psi(V_S)\right] = \sum_{n=3}^{N} C V_S^{n-1} R_n \sin\phi_n \tag{10}$$

$$R(V_S)\cos\left[\Psi(V_S)\right] = 1 + \sum_{n=3}^{N} C V_S^{n-1} R_n \cos\phi_n$$

and

$$C = \frac{1}{a_1 2^{n-1}} \left(\frac{n+1}{2}\right). \tag{11}$$

In fact, $R(V_S)$ represent the AM–AM conversion normalized to a voltage gain of one and $\Psi(V_S)$ represents the AM–PM conversion.

2) Obtaining the Complex Coefficients: To solve for the complex coefficients needed for the CPSR, we have to fit the measured large-signal S_{21} to (10) and (11). If we write the input and output voltage in polar format, S_{21} is defined as

$$\begin{aligned} S_{21} &= \left.\frac{b_2}{a_1}\right|_{Z_L = Z_0} \\ &= \frac{\mathbf{V}_{o,\omega_0}}{\mathbf{V}_i} \\ &= \frac{a_1 V_S R(V_S) e^{j[\omega_0 t + \Psi(V_S)]}}{V_S e^{j\omega_0 t}} \\ &= a_1 R(V_S) e^{j\Psi(V_S)}. \end{aligned} \tag{12}$$

If we combine (10) and (11) and (12), we can write the following system of equations:

$$\begin{aligned} \frac{\mathrm{Im}(S_{21}(V_S))}{a_1} &= R(V_S)\sin\left[\Psi(V_S)\right] \\ &= \sum_{n=3}^{N} C V_S^{n-1} R_n \sin\phi_n \\ \frac{\mathrm{Re}(S_{21}(V_S))}{a_1} &= R(V_S)\cos\left[\Psi(V_S)\right] \\ &= 1 + \sum_{n=3}^{N} C V_S^{n-1} R_n \cos\phi_n. \end{aligned} \tag{13}$$

The complex coefficients $\vec{a}_n = R_n e^{j\phi_n}$ can be determined by solving the system of equations by means of a least square method and a_1 is determined from the measured S_{21} of the first point in the power sweep (see the Appendix). A good fit was obtained up to the compression region for $N = 23$. This is in strong contrast to [6], which only uses a third-order approximation to handle weak nonlinearities.

3) Calculation of IM3: In Section II, we already defined IM3 as the ratio of the signal output at the frequency $2\omega_1 - \omega_2$ to the signal output at the fundamental frequency ω_1. To obtain an expression for IM3, we substitute a two-tone signal $v_i(t) = V_s[\cos(\omega_1 t) + \cos(\omega_2 t)]$ in (7). Equation (14) gives the generalized expression for IM3 as function of input voltage amplitude using the CPSR model and the complex coefficients $\bar{a}_n = R_n e^{j\phi n}$ calculated previously from single-tone data

$$\mathrm{IM3} = 20^* \log \frac{|v_{o,2\omega_1-\omega_2}|}{|v_{o,\omega_1}|}\ [\mathrm{dBc}] \tag{14}$$

where

$$\begin{aligned} &|v_{o,2\omega_1-\omega_2}| \\ &= \left\{\left[\sum_{n=3}^{N} \frac{1}{2^{n-1}} \left(\frac{n}{\frac{n+1}{2}}\right) \left(\frac{n}{\frac{n+3}{2}}\right) V_S^n R_n \cos\phi_n\right]^2 \right. \\ &\quad \left. + \left[\sum_{n=3}^{N} \frac{1}{2^{n-1}} \left(\frac{n}{\frac{n+1}{2}}\right) \left(\frac{n}{\frac{n+3}{2}}\right) V_S^n R_n \sin\phi_n\right]^2\right\}^{1/2} \end{aligned}$$

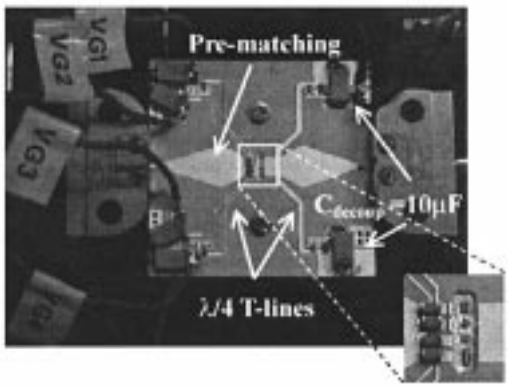

Fig. 10. Hybrid implementation of the linear distributed amplifier concept.

and

$$|v_{o,\omega_1}| = \left\{ \left[a_1 V_S + \sum_{n=3}^{N} \frac{1}{2^{n-1}} \left(\frac{n+1}{2} \right)^2 V_S^n R_n \cos\phi_n \right]^2 + \left[\sum_{n=3}^{N} \frac{1}{2^{n-1}} \left(\frac{n+1}{2} \right)^2 V_S^n R_n \sin\phi_n \right]^2 \right\}^{1/2}.$$

B. Experimental Multivariable Optimization of the Amplifier

We first discuss the features of the novel LDMOS power amplifier and then we explain the linearity optimization routine in more detail. Fig. 10 shows a hybrid implementation of the complete distributed device amplifier. From a matching point-of-view, the parallel-connected transistors can be treated as one single transistor as long as the devices are closely placed together with respect to the wavelength. Pre-matching is included on the circuit board in order to deal with the typically low impedances of LDMOS devices. Shorted $\lambda/4$ transmission lines were used to isolate the RF signal from the bias sources. Supply lines were decoupled using 10-μF surface mount device (SMD) capacitors in order to minimize bias-modulation effects and related memory effects.

The complete amplifier was embedded in the measurement setup, as shown in Fig. 11. This setup consists of an HP 8753E network analyzer to measure S_{21} versus power, a linear booster amplifier to generate the required input power, directional couplers to sense the input and output power, an HP 4145B bias source to bias the individual LDMOS devices, and a computer, which controls the instruments through the HP VEE software. The optimum load was determined manually by slug tuners at $f = 1.95$ GHz using a single 12-mm LDMOS device in class-AB operation. This load condition has been used as reference for the distributed amplifier concept.

The previously discussed CPSR model was implemented in HP VEE, which is a tool capable of performing automatic data acquisition and data processing. The routine was used for the final optimization of the bias parameters of the novel class-AB LDMOS power amplifier [4]. Fig. 12 shows a flowchart of the

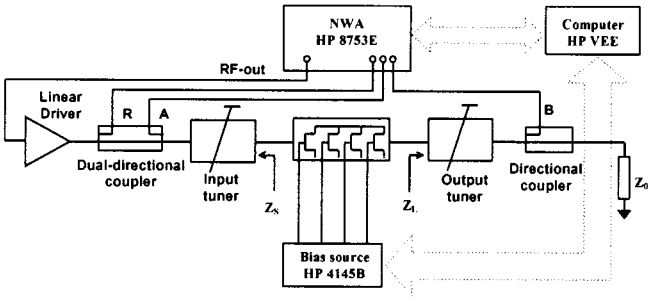

Fig. 11. Computer-controlled measurement setup for optimizing gate-bias voltages for minimum IM3 over a wide power range.

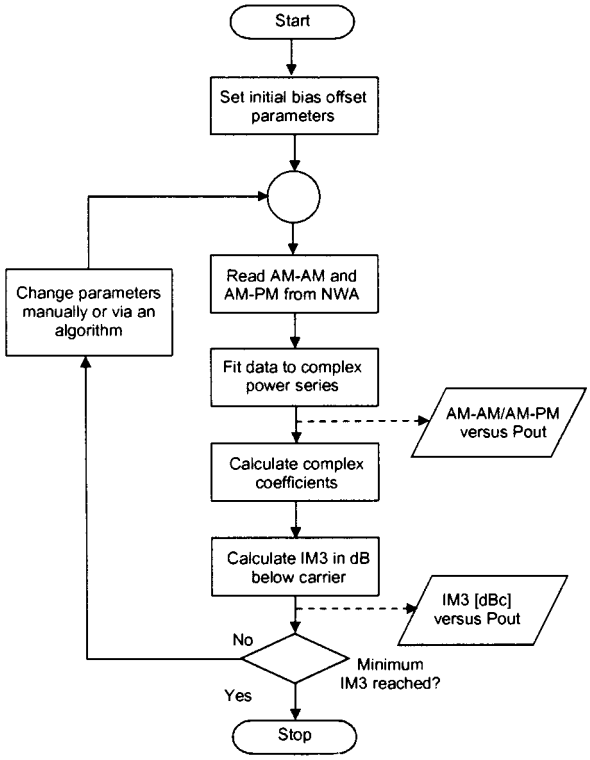

Fig. 12. Flowchart of the linearity optimization routine in HP VEE.

optimization routine. We initially begin with the bias offsets obtained from the analysis in Section III. The offsets are then manually changed until the IM3 versus power is minimized over a wide dynamic range.

Fig. 13(a) and (b) shows the result before and after, respectively, optimizing IM3 versus signal power. Fig. 13(a) shows the case in which the bias offsets were set to zero ($I_{\rm DS} = 60$ mA) and Fig. 13(b) shows the case in which the bias offsets were optimized for maximum flat AM–AM and AM–PM conversion and low IM3 versus power ($I_{\rm DS} = 112$ mA). The dotted curves denote the measured IM3 versus output power using a spectrum analyzer, also for verification of the proposed method. The final offset values were $\Delta V_1 = 0.40$ V, $\Delta V_2 = -0.03$ V, $\Delta V_3 = 0.60$ V, and $\Delta V_4 = -0.30$ V. Note that the drain current is slightly higher than the conventional class-AB operation, but this is because some individual devices are biased closer to class A. We tested the same bias condition ($I_{\rm DS} = 112$ mA) also for the single 12-mm device amplifier and found a worse IM3 behavior in comparison with the optimum class-AB operation

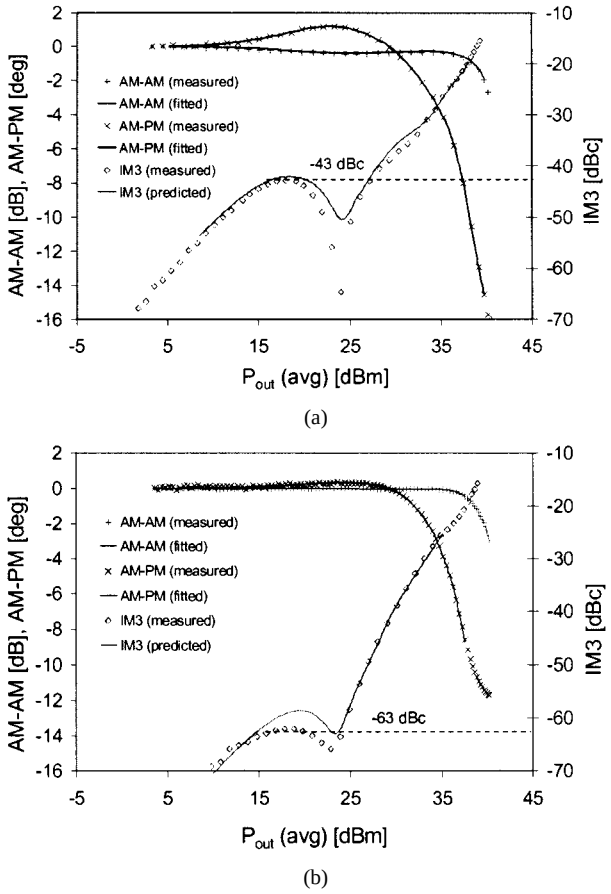

Fig. 13. Measured and predicted IM3, AM–AM, and AM–PM versus output power at $f = 1.95$ GHz in class-AB operation for the: (a) single device and (b) distributed device after optimizing $\Delta V_1 - \Delta V_4$ of the individual devices.

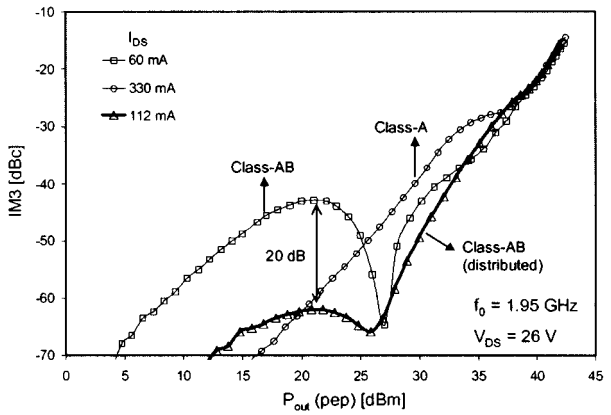

Fig. 14. Measured IM3 versus peak-envelope (pep) output power of the conventional and distributed amplifier design at $f = 1.95$ GHz and $\Delta f = 200$ kHz.

at $I_{\mathrm{DS}} = 60$ mA, which is the IM3 sweet spot for this particular device.

V. Final Results

Fig. 14 shows the improvement in IM3 versus output power for the optimum biased distributed LDMOS-device amplifier together with the optimum biased 12-mm LDMOS-device amplifier in class-A and class-AB operation. The output load at the fundamental was the same for all amplifiers. Note that, in the backoff region, an improvement of 20 dB has been achieved in comparison with a conventional class-AB design. We can also see the disadvantage of using class-A operation with respect to linearity and efficiency at higher output powers. We conclude the experiment with the most rigorous test by applying a WCDMA test signal according to the 3GPP standard [9] at 1.95 GHz. Fig. 15 shows a significant improvement in ACPR of the distributed device amplifier compared to the single device amplifier under class-AB bias condition. In fact, we even outperform the linearity of the amplifier in class-A operation.

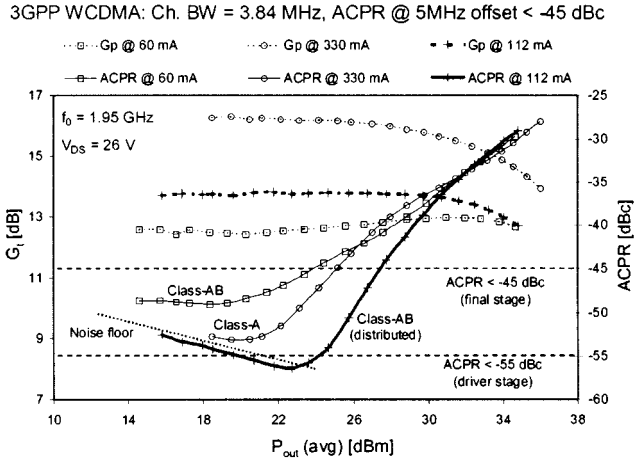

Fig. 15. Measured transducer gain (G_t) and ACPR of a WCDMA signal versus average (avg) output power of the conventional and distributed amplifier design at $f = 1.95$ GHz.

TABLE I
Comparison Results for Different ACPR Specs

	CLASS A SINGLE	CLASS AB SINGLE	CLASS AB DISTR.
I_{DSQ}	330 mA	60 mA	112 mA
Meeting the ACPR =-45 dBc spec. (final stage)			
Pout (dBm)	25.1	23.9	27.4
Eff (%)	3.7	8.0	10.5
Meeting the ACPR =-55 dBc spec. (driver stage)			
Pout	~ 21*	**	24.2
Eff (%)	~ 1.5*	**	6.8
* Within noise margin, ** Does not meet specification			

Table I summarizes the results with respect to the −45 dBc ACPR specification intended for final stages, as well as for a 10-dB better ACPR level intended for driver stages. These results show that by using the distributed amplifier configuration, it is possible to create base-station power amplifiers, which have a significantly better linearity and efficiency than their class-A and class-AB counterparts and require less OPBO from P1dB.

VI. Conclusion

We have demonstrated that the square-law approximated LDMOS power amplifier yields better linearity than conventional class-A or class-AB single-device LDMOS amplifiers. The bias parameters were optimized experimentally for maximum linearity over a large dynamic range by using the CPSR model to predict IM3 versus power. Measurements have demonstrated a linearity improvement over 20 dB in IM3 and

10 dB in ACPR. The concept also allows for operating the distributed LDMOS closer to P1dB, simultaneously providing higher amplifier efficiency and linearity. Therefore, the concept is perfectly suited for both driver and final-stage amplifiers in a WCDMA base-station application.

APPENDIX

In order to calculate the complex coefficients, (13) has to be solved for M values of the input voltage amplitude V_{S}. We do so by writing (13) in matrix form, as shown in (15), at the bottom of this page, in which M corresponds to the number of points in the power sweep, as performed by the network analyzer, N is the order of the complex power series, $\bar{x}$ is the vector containing the desired complex coefficients, and $\bar{b}$ is the vector containing the measured AM–AM and AM–PM versus input voltage. Equation (15) can be solved by using the least square method in matrix notation

$$\bar{x} = \left[A^T \cdot A\right]^{-1} \cdot A^T \cdot \bar{b}. \tag{16}$$

A good fit was obtained up to the compression region for $N = 23$ and $M = 100$.

ACKNOWLEDGMENT

The authors wish to acknowledge the advice and support of F. van Straaten, F. Meeuwsen, and J.-W. van Velzen, Business Line RF Modules, Concept Development and Base Station Development, Philips Semiconductors, Nijmegen, The Netherlands.

$$A(N,M) \cdot \bar{x}(N) = \bar{b}(M) \tag{15}$$

where

$$A(N,M) = \begin{pmatrix} \frac{1}{2^2}\binom{3}{2}\frac{A_1^2}{a_1} & \cdots & \frac{1}{2^{N-1}}\binom{N}{\frac{N+1}{2}}\frac{A_1^{N-1}}{a_1} & 0 & \cdots & 0 \\ 0 & \cdots & 0 & \frac{1}{2^2}\binom{3}{2}\frac{A_1^2}{a_1} & \cdots & \frac{1}{2^{N-1}}\left(\frac{N+1}{2}\right)\frac{A_1^{N-1}}{a_1} \\ \frac{1}{2^2}\binom{3}{2}\frac{A_2^2}{a_1} & \cdots & \frac{1}{2^{N-1}}\left(\frac{N+1}{2}\right)\frac{A_2^{N-1}}{a_1} & 0 & \cdots & 0 \\ 0 & \cdots & 0 & \frac{1}{2^2}\binom{3}{2}\frac{A_2^2}{a_1} & \cdots & \frac{1}{2^{N-1}}\left(\frac{N+1}{2}\right)\frac{A_2^{N-1}}{a_1} \\ \vdots & & \vdots & \vdots & & \vdots \\ \frac{1}{2^2}\binom{3}{2}\frac{A_M^2}{a_1} & \cdots & \frac{1}{2^{N-1}}\left(\frac{N+1}{2}\right)\frac{A_M^{N-1}}{a_1} & 0 & \cdots & 0 \\ 0 & \cdots & 0 & \frac{1}{2^2}\binom{3}{2}\frac{A_M^2}{a_1} & \cdots & \frac{1}{2^{N-1}}\left(\frac{N+1}{2}\right)\frac{A_M^{N-1}}{a_1} \end{pmatrix}$$

$$\bar{x}(N) = \begin{pmatrix} R_3 \sin\phi_3 \\ \vdots \\ R_N \sin\phi_N \\ R_3 \cos\phi_3 \\ \vdots \\ R_N \cos\phi_N \end{pmatrix}$$

and

$$\bar{b}(M) = \begin{pmatrix} R(A_1)\sin\Psi(A_1) \\ R(A_1)\cos\Psi(A_1) - 1 \\ R(A_2)\sin\Psi(A_2) \\ R(A_2)\cos\Psi(A_2) - 1 \\ \vdots \\ \vdots \\ R(A_M)\sin\Psi(A_M) \\ R(A_M)\cos\Psi(A_M) - 1 \end{pmatrix}$$

REFERENCES

[1] J.-J. Bouny, "Advantages of LDMOS in high power linear amplification," *Microwave Eng. Eur.*, pp. 37–40, Apr. 1996.

[2] S. Cripps, *RF Power Amplifiers for Wireless Communications*. Norwood, MA: Artech House, 1999.

[3] P. B. Kennington, *High-Linearity RF Amplifier Design*. Norwood, MA: Artech House, 2000.

[4] M. P. van der Heijden, H. C. de Graaff, L. C. N. de Vreede, J. R. Gajadharsing, and J. N. Burghartz, "Ultra-Linear distributed class-AB LDMOS power amplifier for base stations," in *IEEE MTT-S Int. Microwave Symp. Dig.*, May 2001, pp. 1363–1365.

[5] M. P. van der Heijden, J. R. Gajadharsing, B. Rejaei, and L. C. N. de Vreede, "Linearity optimization of a distributed base station amplifier using an automated high-speed measurement protocol," in *IEEE MTT-S Int. Microwave Symp. Dig.*, May 2001, pp. 1679–1682.

[6] T. Nojima, "Nonlinear compensation technologies for microwave power amplifiers in radio communication systems," *IEICE Trans. Electron.*, vol. E82-C, no. 5, May 1999.

[7] P. J. Gonzalez, L. F. Herran, J. A. Garcia, T. Fernandez, A. Tazon, A. Mediavilla, and J. L. Garcia, "Detecting IMD sweet spots in LDMOS devices through an accurate nonlinear characterization," in *Eur. Microwave Conf.*, vol. 1, Oct. 2000, pp. 105–107.

[8] D. R. Webster, D. G. Haigh, and A. E. Parker, "Novel circuit synthesis technique using short channel GaAs FET's giving reduced intermodulation distortion," in *IEEE Int. Circuits Syst. Symp.*, Seattle, WA, Apr.–May 1995, pp. 1348–1351.

[9] *3GPP—3rd Generation Partnership Project*, Tech. Spec. Group Radio Access Networks, Base Station Confirmation Testing (FDD), 1999.

[10] N. B. de Carvalho and J. C. Pedro, "Large signal IMD sweet spots in microwave power amplifiers," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1999, pp. 517–520.

[11] D. R. Webster, J. Scott, and D. G. Haigh, "Control of circuit distortion by the derivative superposition method," *IEEE Microwave Guided Wave Lett.*, vol. 6, pp. 123–125, Mar. 1996.

[12] B. Kim, J.-S. Ko, and K. Lee, "A new linearization technique for MOSFET RF amplifier using multiple gated transistors," *IEEE Microwave Guided Wave Lett.*, vol. 10, pp. 371–373, Sept. 2000.

[13] *Maple V Language Reference Manual*. New York: Springer-Verlag, 1991.

[14] A. Katz and R. Dorval, "Evaluation and correction of time dependent amplifier nonlinearity," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1996, pp. 839–842.

[15] N. B. de Carvalho and J. C. Pedro, "Two-tone IMD asymmetry in microwave power amplifiers," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 2000, pp. 445–448.

Mark P. van der Heijden (S'98) was born in Benthuizen, The Netherlands, in 1976. He received the B.S. degree in electrical engineering from The Hague Polytechnic, The Hague, The Netherlands, in 1998, the MTD degree (Masters degree of technological design) in microelectronics from the Delft University of Technology, Delft, The Netherlands, in 2000, and is currently working toward the Ph.D. degree in electrical engineering at the Delft University of Technology.

In 1988, he joined the Laboratory of Electronic Components, Technology and Materials, Department of Information Technology and Systems, Delft University of Technology. From 1998 to 2000, he was involved with isothermal characterization of MOST devices and power-amplifier design for linearity. His research interests include design of RF building blocks for linearity and dynamic range.

Henk C. de Graaff (M'92) was born in Rotterdam, The Netherlands, in 1933. He received the M.Sc. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1956, and the Ph.D. degree from the University of Technology, Eindhoven, The Netherlands, in 1975.

In 1964, he joined Philips Research Laboratories, Eindhoven, The Netherlands, where he was involved with thin-film transistors, MOST, bipolar devices, and material research on polycrystalline silicon. His current field of interest is device modeling for circuit simulation. In November 1991, he retired from Philips Research Laboratories. He was a consultant to the University of Twente, Twente, The Netherlands, until 1996. He currently consults for the Technical University of Delft, The Netherlands.

Leo C. N. de Vreede (M'00) was born in Delft, The Netherlands, in 1965. He received the B.S. degree in electrical engineering from The Hague Polytechnic, The Hague, The Netherlands, in 1988, and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 1996.

In 1988, he joined the Laboratory of Telecommunication and Remote Sensing Technology, Department of Electrical Engineering, Delft University of Technology. From 1988 to 1990, he was involved in the characterization and physical modeling of ceramic multilayer capacitor (CMC) capacitors. From 1990 to 1996, he was involved with the modeling and design aspects of high-frequency silicon integrated circuits for wide-band communication systems. In 1996, he became an Assistant Professor with the Delft University of Technology. He has been involved with the nonlinear distortion behavior of bipolar transistors at the device physics and compact-model levels, as well as the circuit level with the Delft Institute of Microelectronics and Submicron Technology (DIMES). In Winter 1998–1999, he was a guest of the High-Speed Device Group, University of San Diego, CA. In 1999, he became an Associate Professor with the Microwave Components Group, Delft University of Technology. His current interest is technology optimization and circuit design for improved RF performance and linearity.

John R. Gajadharsing was born in Paramaribo, Suriname, in December 1959. He graduated from the Technical Institute, Arnhem, The Netherlands, in 1985.

In 1985, he joined Business Line RF Modules, Philips Semiconductors Nijmegen, The Netherlands, where he has been involved with RF power device technologies. He is currently active in advanced development of RF power concepts for base-stations transmitters.

Mr. Gajadharsing is a member of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) Administrative Committee (AdCom) and the IEEE Communications Society.

Joachim N. Burghartz (M'90–SM'92–F'02) received the Dipl. Ing. degree from the Technische Hochschule Aachen, Aachen, Germany, in 1982, and the Ph.D. degree from the University of Stuttgart, Stuttgart, Germany, in 1987, both in electrical engineering.

From 1982 to 1987, he was with the University of Stuttgart, where he developed sensors with integrated signal conversion with a special focus on magnetic-field sensors. From 1987 to 1998, he was with the IBM T. J. Watson Research Center, Yorktown Heights, NY. His earlier research work at IBM included applications of Si and SiGe epitaxial growth in high-speed transistor design and integration processes, in which he was a member of the pioneering team that invented and developed IBM's SiGe technology. From 1992 to 1994, he was a Project Leader involved with the development of a 0.15-μm CMOS at IBM Microelectronics, East Fishkill, NY. From 1994 to 1998, he concentrated on the design of circuit building blocks for SiGe RF front-ends, with a special interest in high-quality passive components in silicon technology. He has been driving the integration and optimization of spiral inductors on silicon substrates. In November 1998, he became a Full Professor with teaching responsibilities in electrical engineering and microelectronic research with the Delft Institute of Microelectronics and Submicron Technology (DIMES), Delft University of Technology, Delft, The Netherlands. With DIMES, he has extended his research in RF silicon technology to aspects ranging from novel materials to RF circuits. Since 1999, he has lead the DIMES research theme "High-Frequency Silicon Technologies for Communications." In March 2001, he became the Scientific Director of DIMES. He has authored and coauthored numerous technical papers, over 100 publications in refereed journals and conference proceedings, and holds 12 U.S. patents.

Prof. Burghartz is a member of the Program Committees of the technical conferences of the International Electron Devices Meeting (IEDM), European Solid-State Device Research Conference (ESSDERC), and Bipolar/BiCMOS Circuits and Technology Meeting (BCTM). He was the BCTM general chairman in 2000.